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Question Paper Code : 71725

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2017.

Third Semester

Electronics and Communication Engineering

EC 6302 — DIGITAL ELECTRONICS

(Common to Mechatronics Engineering, Robotics and Automation Engineering)

(Regulations 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the given decimal numbers to their binary equivalent 108.364, 268.025.
2. Show how to connect NAND gates to get an AND gate and OR gate?
3. Draw the truth table and the logic circuit of half adder.
4. Compare the function of Decoder and Encoder.
5. Derive the characteristic equation of a D flip flop.
6. What is the primary disadvantage of asynchronous counter?
7. How does ROM retain information?
8. Differentiate between PAL and PLA.
9. What are the steps for the analysis of asynchronous sequential circuit?
10. What is the significance of state assignment?

PART B — (5 × 13 = 65 marks)

11. (a) A using K map find the MSP form of F = (0-3, 12-15) + d(7, 11). (13)

Or

(b) (i) State and prove De Morgon's theorem. (3)

(ii) Find a MinSOP and MinPOS for

$F = \bar{b}\bar{c}d + bcd + ac\bar{d} + \bar{a}\bar{b}c + \bar{a}b\bar{c}d$. (10)

12. (a) Implement $Y = (A + C)(A + \overline{D})(A + B + \overline{C})$ using NOR gates only. (13)

Or

(b) (i) Why does a good logic designer minimize the use of NOT gates? (3)

(ii) Show that if all the gates in a two-level AND-OR gate networks are replaced by NAND gates the output function does not change. (10)

13. (a) Design and explain the working of a synchronous mod-3 counter. (13)

Or

(b) Using SR flipflops design a parallel counter which counts in the sequence 000, 111, 101, 110, 001, 010, 000,... (13)

14. (a) (i) Compare static RAM and Dynamic RAM. (3)

(ii) Implement the switching functions. (10)

$z1 = a\overline{b}\,\overline{d}e + \overline{a}\,\overline{b}\overline{c}\,\overline{e} + bc + de$

$z2 = \overline{a}\,\overline{c}e$

$z3 = bc + de + \overline{c}\,\overline{d}\,\overline{e} + bd$ and

$z4 = \overline{a}\,\overline{c}e + ce$ using a5*8*4 PLA.

Or

(b) (i) Distinguish between Boolean addition and binary addition. (3)

(ii) Design a combinational circuit using a ROM that accepts a 3 bit number and generates an output binary number equal to the square of the given number. (10)

15. (a) (i) Summarize the design procedure for a synchronous sequential circuit. (10)

(ii) Derive the state table of a serial binary adder. (3)

Or

(b) What is the objective of state assignment in a asynchronous circuit? Give the hazard free realization for the Boolean function f(A, B, C, D) = M(0, 2, 6, 7, 8, 10, 12). (13)

PART C — (1 × 15 = 15 marks)

16. (a) A sequential machine has one input line where 0's and 1's are being incident. The machine has to produce a output of '1' only when exactly two '0's are followed by a '1' or exactly two '1's are followed by a '0'. Using any state assignment and JK flipflop, synthesize the machine. (15)

Or

(b) Find an expression for the following function using Quiue McCluscky method F = (0, 2, 3, 5, 9, 11, 13, 14, 16, 18, 24, 26, 28, 30). (15)